Amendments to the Claims

Please amend the claims to read as follows:

1-9 (Canceled)

10. (Currently Amended) A method for injection of fault values at selected fault injection locations of a programmable circuit device, comprising:

storing and updating fault injection selection data in a first register in response to a first clock signal;

scanning and storing fault injection values in a second register in response to a second clock signal independent of the first clock signal, wherein the fault injection values comprise either stuck-at fault injection values or stuck-on fault injection values for corresponding fault injection locations of the programmable circuit device; and

updating the fault injection selection data and the fault injection values at the selected fault injection locations of the programmable circuit device, while the selected fault injection locations are controlled by the data in the first register and by the fault injection values in the second register instead of by system logic of the programmable circuit device.

11. (Currently Amended) The method of claim 10, and further comprising:

injecting stuck-on fault injection values on selected pins ~~of the~~ comprising the selected fault injection locations.

12. (Currently Amended) The method of claim 10, and further comprising:

injecting stuck-at fault injection values on selected pins ~~of the~~ comprising the selected fault injection locations.

13. (Currently Amended) The method of claim 10, and further comprising:

injecting stuck-on fault injection values on selected pins ~~of the~~ comprising the selected fault injection locations; and

injecting stuck-at fault injection values on selected pins ~~of the~~ comprising the selected fault injection locations

14. (Currently Amended) The method of claim 10, and further comprising:

injecting stuck-on fault injection values on selected pins ~~of the~~ comprising the selected fault injection locations while the programmable circuit device is mounted on a circuit board, to test for vector verification of circuitry of the circuit board.

15. (Currently Amended) The method of claim 10, and further comprising:

injecting stuck-at fault injection values on selected pins ~~of the~~ comprising the selected fault injection locations while the programmable circuit device is mounted on a circuit board, to test for vector verification of circuitry of the circuit board.

16. (Currently Amended) A method for injection of fault values at selected fault injection locations of a programmable circuit device, comprising:

storing and updating fault injection selection data in a first register;

scanning and storing fault injection values in a second register; and

updating the fault injection selection data and the fault injection values at the selected fault injection locations of the programmable circuit device, while the selected fault injection locations are controlled by the data in the first register and by the values in the second register instead of by system logic of the circuit device; ~~The method of claim 10, and further comprising:~~

injecting stuck-on fault injection values on selected first pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the first pins, while the programmable circuit device is mounted on a circuit board, to test for vector routing verification of the circuit board; and

injecting stuck-at fault injection values on selected second pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the second pins, while the programmable circuit device is mounted on a circuit board, to test for vector routing verification of the circuit board.

17. (Currently Amended) A method for injection of fault values at selected fault injection locations of a programmable circuit device, comprising:

storing and updating fault injection selection data in a first register;

scanning and storing fault injection values in a second register; and

updating the fault injection selection data and the fault injection values at the selected fault injection locations of the programmable circuit device, while the selected fault injection locations are controlled by the data in the first register and by the values in the second register instead of by system logic of the circuit device; ~~The method of claim 10, and further comprising:~~

injecting stuck-on fault injection values on selected first pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the first pins, while the programmable circuit device is mounted on a circuit board being tested by verification test software, to test for verification of a new algorithm of the software; and

injecting stuck-at fault injection values on selected second pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the second pins, while the programmable circuit device is mounted on a circuit board being tested by verification test software, to test for verification of a new algorithm of the software.

18. (Original) The method of claim 10, and further comprising: injecting one or more of the fault injection values at an internal register in the system logic of the circuit device.

19. (New) The method of claim 16, and further comprising:

storing and updating fault injection selection data in the first register in response to a first clock signal;

scanning and storing fault injection values in a second register in response to a second clock signal independent of the first clock signal, wherein the fault injection

values comprise either stuck-at fault injection values or stuck-on fault injection values for corresponding fault injection locations of the programmable circuit device.

20. (New) The method of claim 17, and further comprising:

storing and updating fault injection selection data in the first register in response to a first clock signal;

scanning and storing fault injection values in a second register in response to a second clock signal independent of the first clock signal, wherein the fault injection values comprise either stuck-at fault injection values or stuck-on fault injection values for corresponding fault injection locations of the programmable circuit device.